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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,661	05/14/2001	Masahiro Tanaka	208546US2	6508
22850	7590	05/18/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			DIAZ, JOSE R	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	Application No. 09/853,661	Applicant(s) TANAKA, MASAHIRO	
	Examiner José R. Díaz	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 February 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,2,4,5,16-18,27-30 and 35-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,4,5,16-18,27-30 and 35-38 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-2, 4-5, 16-18, 27-30 and 35-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (US Pat. No. 4,893,165) in view of Sakurai (US Pat. No. 5,200,632).

Regarding claim 1, Miller et al. teaches an electrode contact section incorporated in a semiconductor device; comprising:

a first conductivity type (N-type) semiconductor substrate (2) (see fig. 2);

a second conductivity type impurity layer (15) formed in one surface of the semiconductor substrate (see fig. 2) and having a peak of an impurity concentration at a point of more than 0.2  $\mu\text{m}$  and not more than 1.0  $\mu\text{m}$  from the one surface of the semiconductor substrate (a thickness of less than 1  $\mu\text{m}$ , preferably of about 0.1  $\mu\text{m}$ ) [col.2, lines 64-66];

a first electrode (14) formed on the impurity layer (see fig. 2); and

a second electrode (10) formed at another surface of the semiconductor substrate for allowing a current to flow between the first and second electrodes (see fig. 2).

However, Miller et al. fails to teach a second conductivity type contact layer formed in the impurity layer and having a peak of an impurity concentration at a point of not more than 0.2  $\mu\text{m}$  from the one surface of the semiconductor substrate, the contact layer being thinner than the impurity layer and the peak of the impurity concentration of the contact layer being higher than that of the impurity layer; and a first electrode formed on the contact layer.

Sakurai teaches that it is well known in the art to include a second conductivity type contact layer (1) formed in the impurity layer (12), the contact layer (1) being thinner than the impurity layer (12) and the peak of the impurity concentration of the contact layer ( $P^+$ ) being higher than that of the impurity layer ( $P^-$ ); and a first electrode (10) formed on the contact layer (1).

With regards to the limitation that the contact layer has a peak of an impurity concentration at a point of not more than 0.2  $\mu\text{m}$  from the one surface of the semiconductor substrate, Sakurai teaches that the depth of the contact layer (1) can be modified as desired [col. 6, lines 59-60]. Thus, it is considered that the depth of the contact layer can be modified to be less than the depth of the impurity layer (15) taught by Miller et al. (col. 2, lines 64-66 of Miller et al.), in this case "less than one micrometer", if so desired. As such, Sakurai makes obvious the uses of a shallow contact layer having a depth of not more than about 0.2  $\mu\text{m}$ .

Miller et al. and Sakurai are analogous because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a second conductivity type

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contact layer in the impurity layer and having a peak of an impurity concentration at a point of not more than 0.2  $\mu\text{m}$  from the one surface of the semiconductor substrate, the contact layer being thinner than the impurity layer and the peak of the impurity concentration of the contact layer being higher than that of the impurity layer; and a first electrode formed on the contact layer. The motivation for doing so, as taught by Sakurai, is improving the efficiency of the electron re-injection (col. 5, lines 50-53). Therefore, it would have been obvious to combine Sakurai with Miller et al. to obtain the invention of claims 1-2, 4-5, 16-18, 27-30 and 35-38.

Regarding claims 2 and 17, Sakurai teaches that the impurity layer (12) is provided for carrier injection from the impurity layer to the semiconductor substrate (col. 7, lines 30-35); and the contact layer (1) is provided for reducing a contact resistant between the first electrode and the impurity layer and not for carrier injection (col. 8, lines 33-36).

Regarding claim 4, Miller et al. teaches an IGBT device (abstract).

Regarding claims 5 and 18, Miller et al. teaches that the impurity layer (15) is formed in the entire one surface of the semiconductor substrate (see fig. 2).

Regarding claim 16, Miller et al. and Sakurai, as stated in the rejection of claim 1 above, teaches the claimed device. In addition, Miller et al. teaches an IGBT device comprising:

- a second conductivity type base region (5) formed in one surface of the semiconductor substrate (2) (see fig. 2);

- a first conductivity type impurity region (6) formed in the base region (see fig. 2);

a gate electrode (8) connected to the base region via an insulation film (7) (see fig. 2).

Regarding claims 27, 29, 35 and 37, Miller et al. teaches that the impurity layer (15) has a thickness of less than 1  $\mu\text{m}$ , preferably of about 0.1  $\mu\text{m}$  (col. 2, lines 64-66).

Regarding claims 28, 30, 36 and 38, Sakurai, as stated before, teaches a thin contact layer (1) having a depth that can be modified as desired (col. 6, lines 59-60). Thus, it is considered that the depth of the contact layer can be modified to be less than the depth of the impurity layer (15) taught by Miller et al. (col. 2, lines 64-66 of Miller et al.), in this case "less than one micrometer", if so desired. As such, Sakurai makes obvious the uses of a shallow contact layer having a depth of about 0.2  $\mu\text{m}$  and/or 0.16  $\mu\text{m}$ .

### ***Response to Arguments***

3. Applicant's arguments with respect to claims 1-2, 4-5, 16-18, 27-30 and 35-38 have been considered but are moot in view of the new ground of rejection.

4. In addition and with regards to the claimed ranges of depth, it is noted that during the patent prosecution of the instant application, applicant relied on the claimed depth to argue the rejections presented by the examiner. However, as set forth above, the examiner considers that the claimed ranges are obvious and as such, fail to patentably distinguish the claimed invention from the prior art. If applicant still considers the claimed ranges to be unobvious, the examiner hereby advises applicant to file an affidavit under 37 CFR 1.132 showing evidence of unexpected results.

### ***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kirihata (US Pat. No. 5,360,984) teaches an IGBT having P<sup>+</sup> regions (17) in a P-type layer (8) (see abstract).

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

### ***Correspondence***


Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD  
5/16/05

  
**GEORGE ECKERT**  
**PRIMARY EXAMINER**